FIG.1

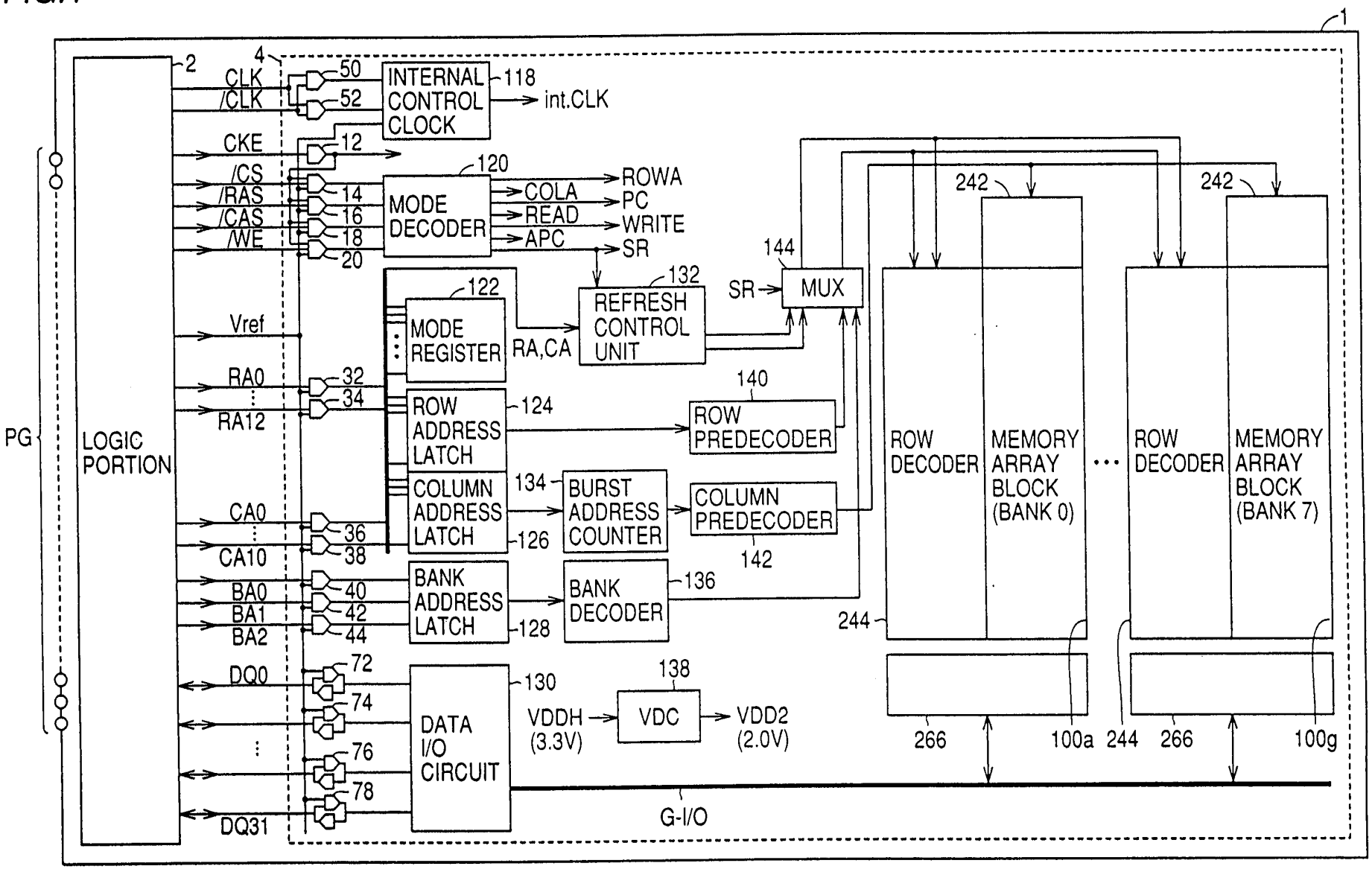
1
2
4
PG
LOGIC PORTION
CLK
/CLK
50
52
INTERNAL CONTROL CLOCK
118
int.CLK
CKE
12
/CS
/RAS
/CAS
/WE
14
16
18
20
120
MODE DECODER
COLA
READ
APC
ROWA
PC
WRITE
SR
122
MODE REGISTER
RA,CA
132
REFRESH CONTROL UNIT
144
SR
MUX
Vref
RA0
RA12
32
34
ROW ADDRESS LATCH
124
140
ROW PREDECODER
CA0
CA10
36
38
COLUMN ADDRESS LATCH
126
134
BURST ADDRESS COUNTER
COLUMN PREDECODER
142
BA0
BA1
BA2
40
42
44
BANK ADDRESS LATCH
128
BANK DECODER
136
DQ0
DQ31
72
74
76
78
DATA I/O CIRCUIT
130
138
VDDH (3.3V)
VDC
VDD2 (2.0V)
G-I/O
242
242
244
ROW DECODER
MEMORY ARRAY BLOCK (BANK 0)
ROW DECODER
MEMORY ARRAY BLOCK (BANK 7)
266
100a
244
266
100g

FIG.2

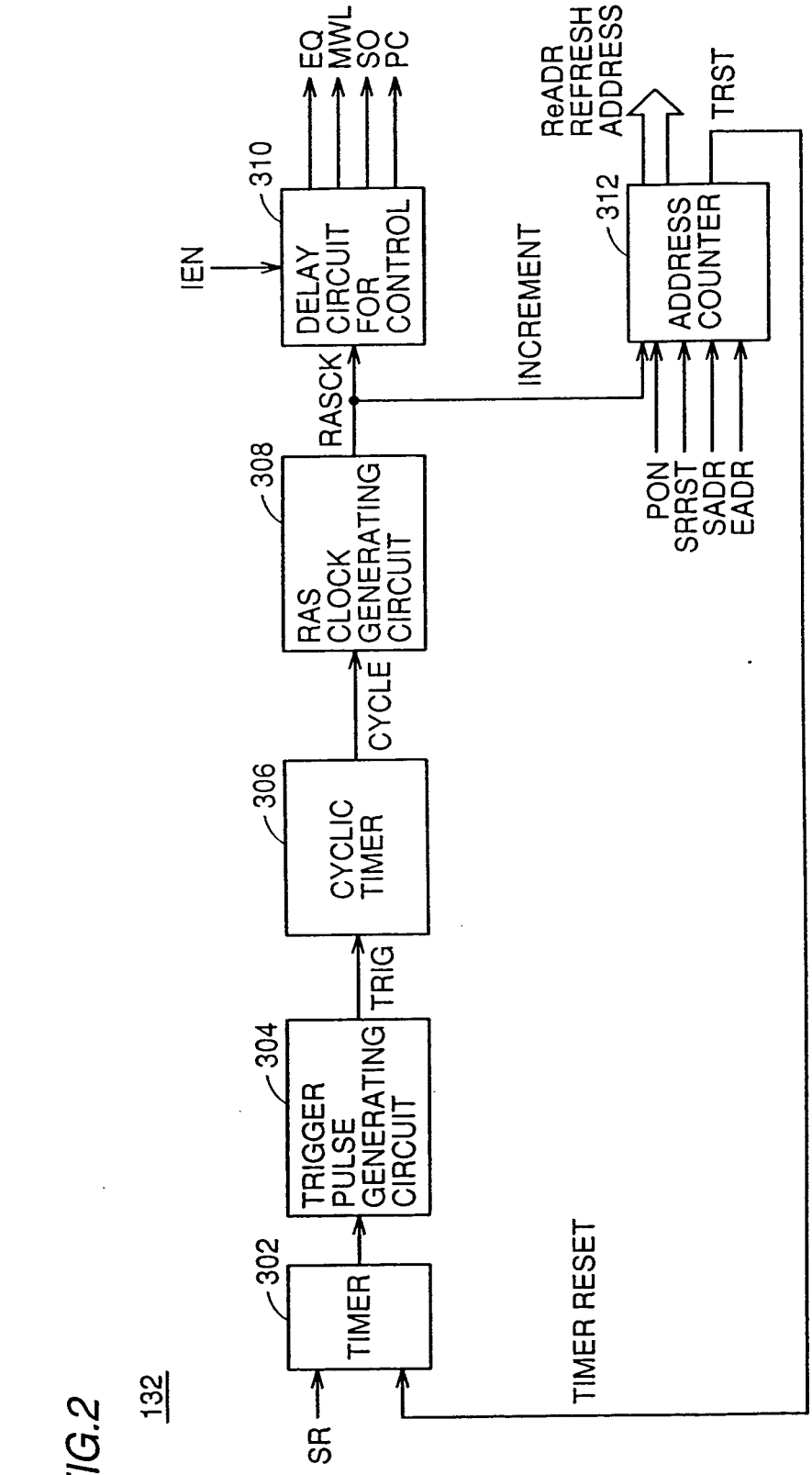
132
SR
302
TIMER
304
TRIGGER PULSE GENERATING CIRCUIT
TRIG
306
CYCLIC TIMER
CYCLE
308
RAS CLOCK GENERATING CIRCUIT
RASCK
310
DELAY CIRCUIT FOR CONTROL
IEN
EQ
MWL
SO
PC
TIMER RESET
INCREMENT
312
ADDRESS COUNTER
PON
SRRST
SADR
EADR
ReADR
REFRESH
ADDRESS
TRST

FIG.3

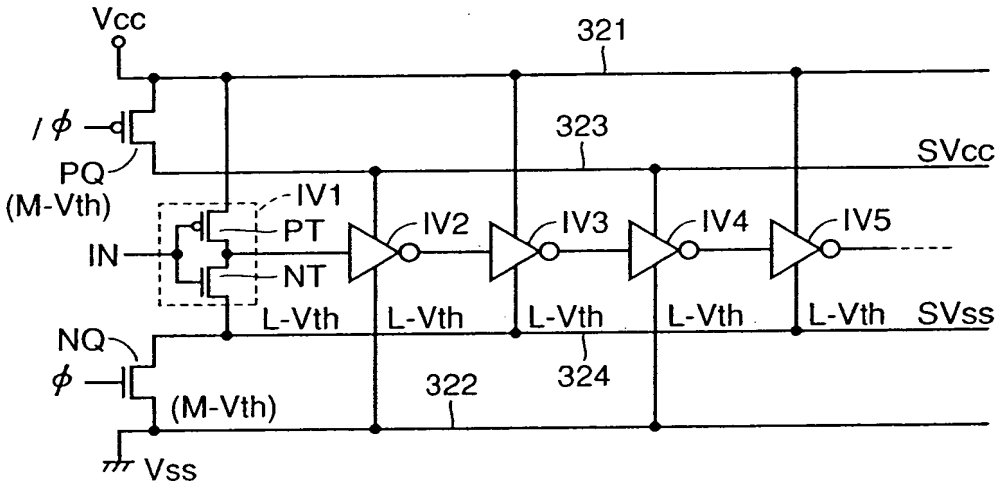
Vcc
321
/ϕ
323
SVcc
PQ
(M-Vth)
IV1
PT
IV2
IV3
IV4
IV5
IN
NT
L-Vth
L-Vth
L-Vth
L-Vth
L-Vth
SVss
NQ
ϕ
322
324
(M-Vth)
Vss

FIG.4

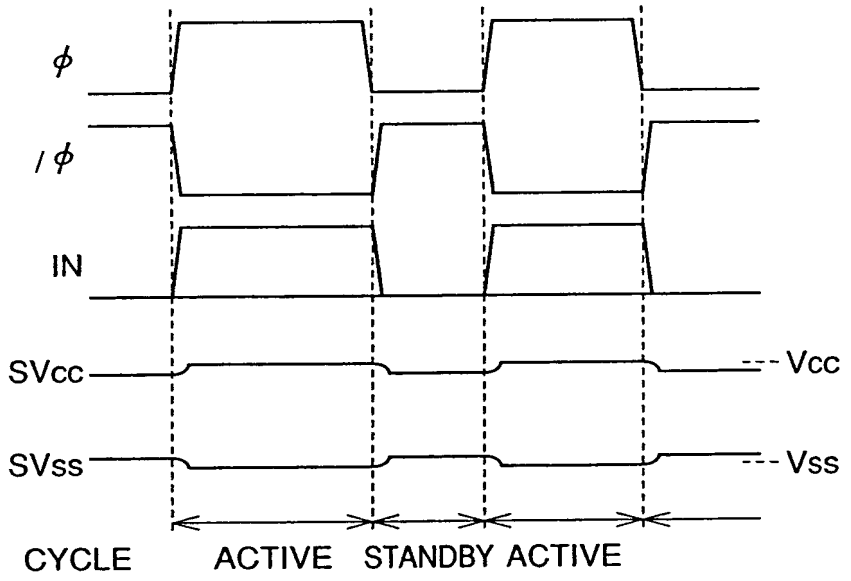
ϕ
/ϕ
IN
SVcc
Vcc
SVss
Vss
CYCLE
ACTIVE
STANDBY
ACTIVE

FIG.5

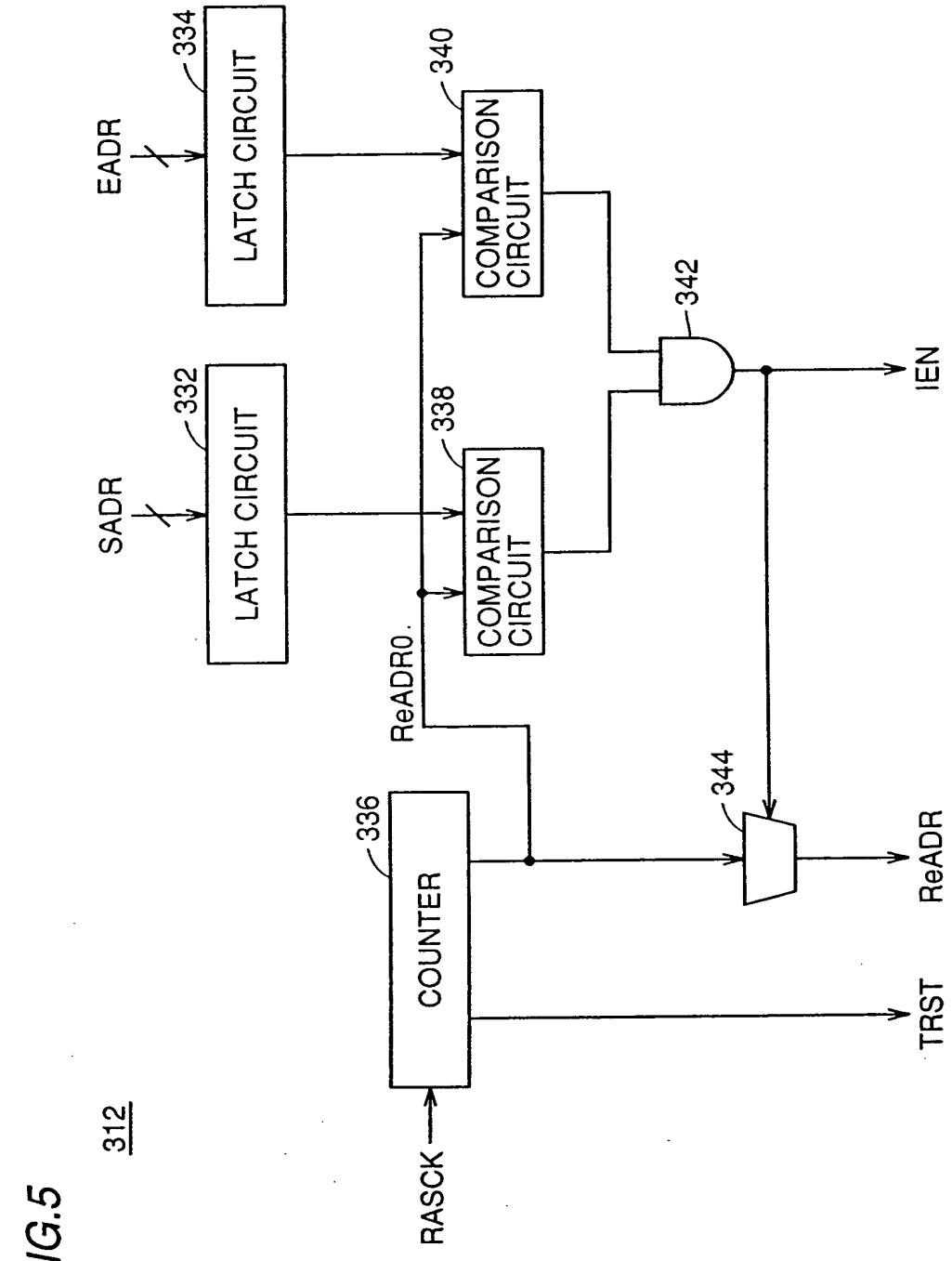
312
EADR
334
LATCH CIRCUIT
340
COMPARISON CIRCUIT
SADR
332
LATCH CIRCUIT
338
COMPARISON CIRCUIT
342
IEN
ReADR0
336
COUNTER
344
ReADR
RASCK
TRST

FIG.6

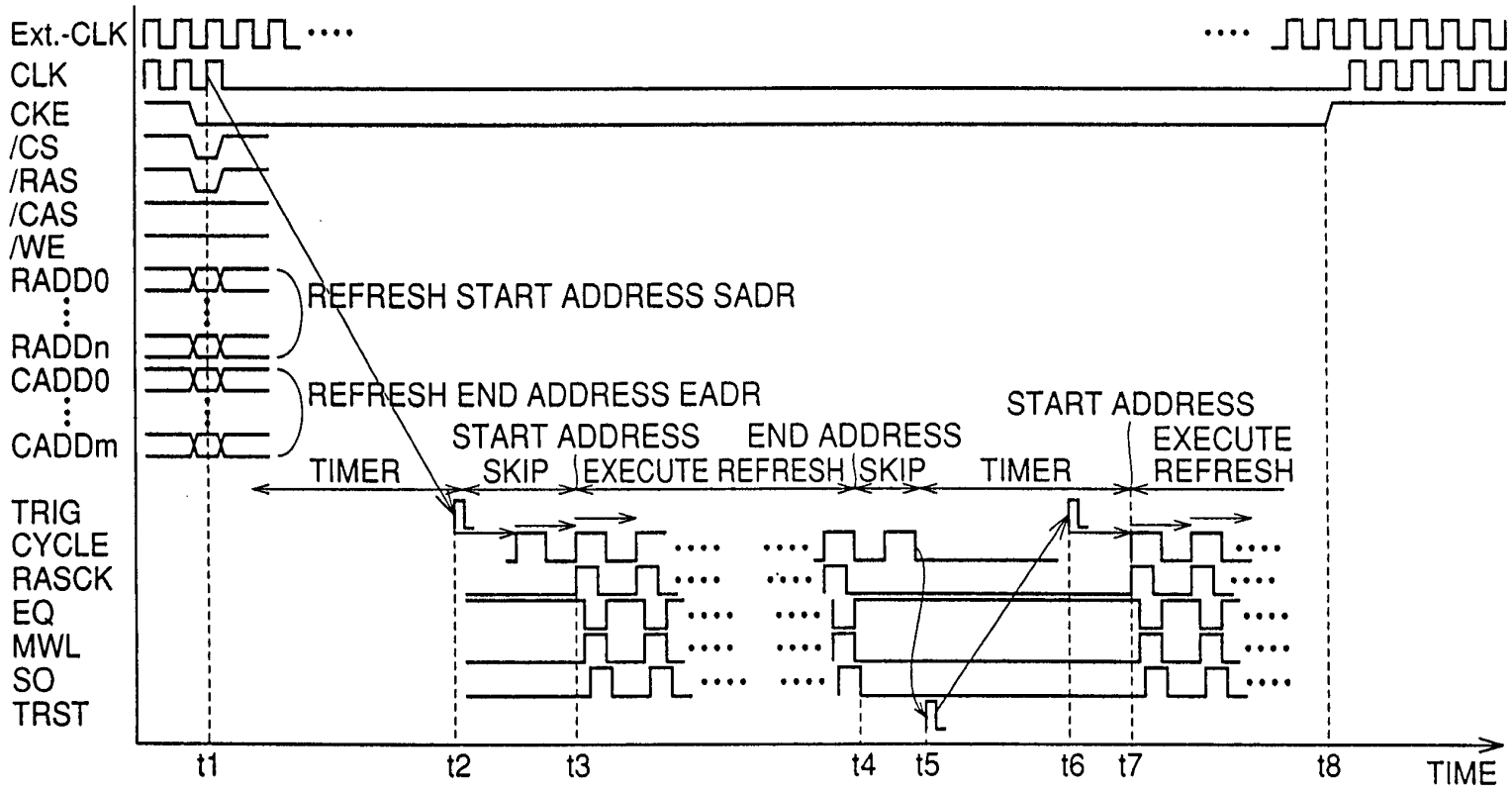
Ext.-CLK
CLK
CKE
/CS
/RAS
/CAS
/WE
RADD0
RADDn
CADD0
CADDm
TRIG
CYCLE
RASCK
EQ
MWL
SO
TRST
REFRESH START ADDRESS SADR
REFRESH END ADDRESS EADR
TIMER
START ADDRESS SKIP
EXECUTE REFRESH
END ADDRESS SKIP
TIMER
START ADDRESS EXECUTE REFRESH
t1
t2
t3
t4
t5
t6
t7
t8
TIME

FIG.7

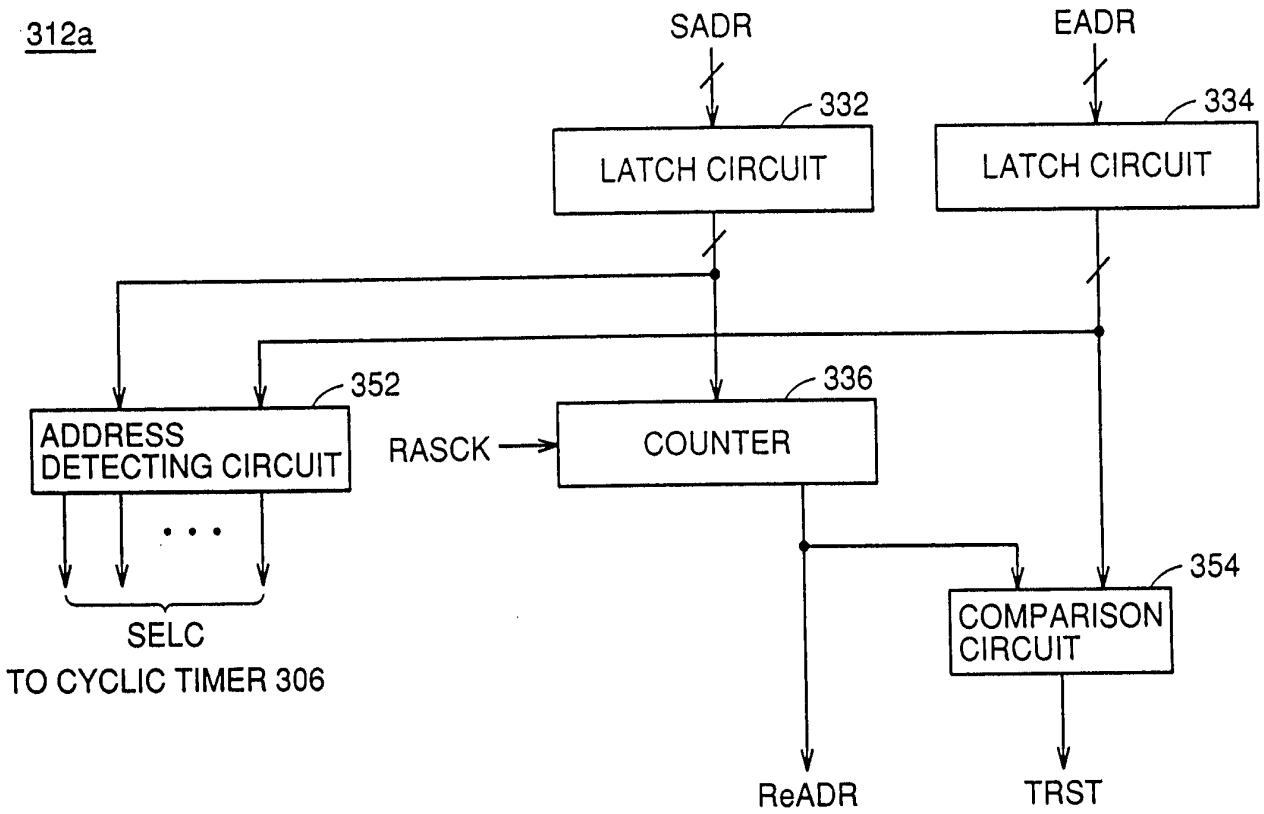
312a
SADR
EADR
332
334
LATCH CIRCUIT
LATCH CIRCUIT
352
336
ADDRESS DETECTING CIRCUIT
RASCK
COUNTER
354
COMPARISON CIRCUIT
SELC
TO CYCLIC TIMER 306
ReADR
TRST

FIG.8

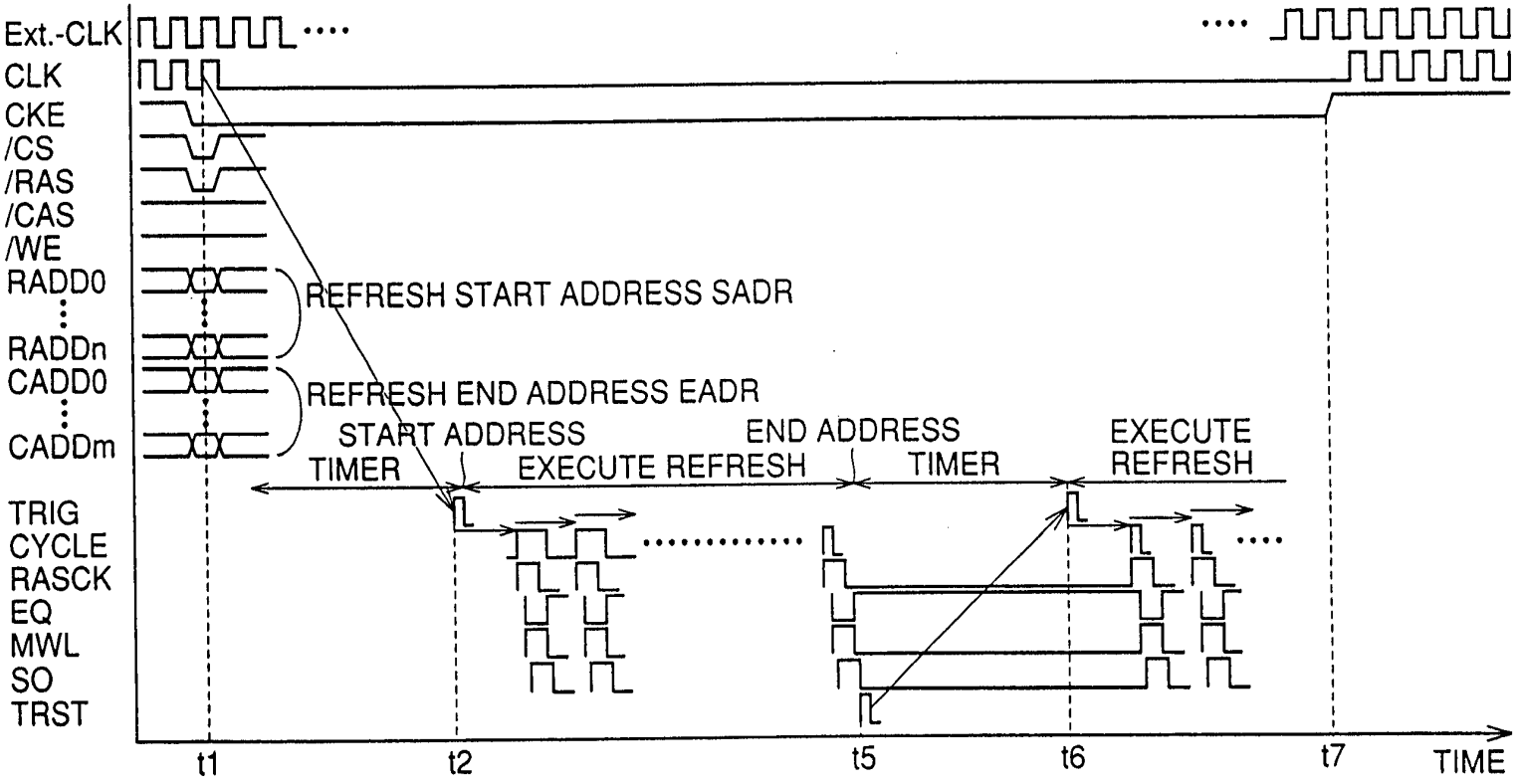
Ext.-CLK
CLK
CKE
/CS
/RAS
/CAS
/WE
RADD0
RADDn
CADD0
CADDm
REFRESH START ADDRESS SADR
REFRESH END ADDRESS EADR
START ADDRESS TIMER
EXECUTE REFRESH
END ADDRESS TIMER
EXECUTE REFRESH
TRIG
CYCLE
RASCK
EQ
MWL
SO
TRST
t1
t2
t5
t6
t7
TIME

FIG.9

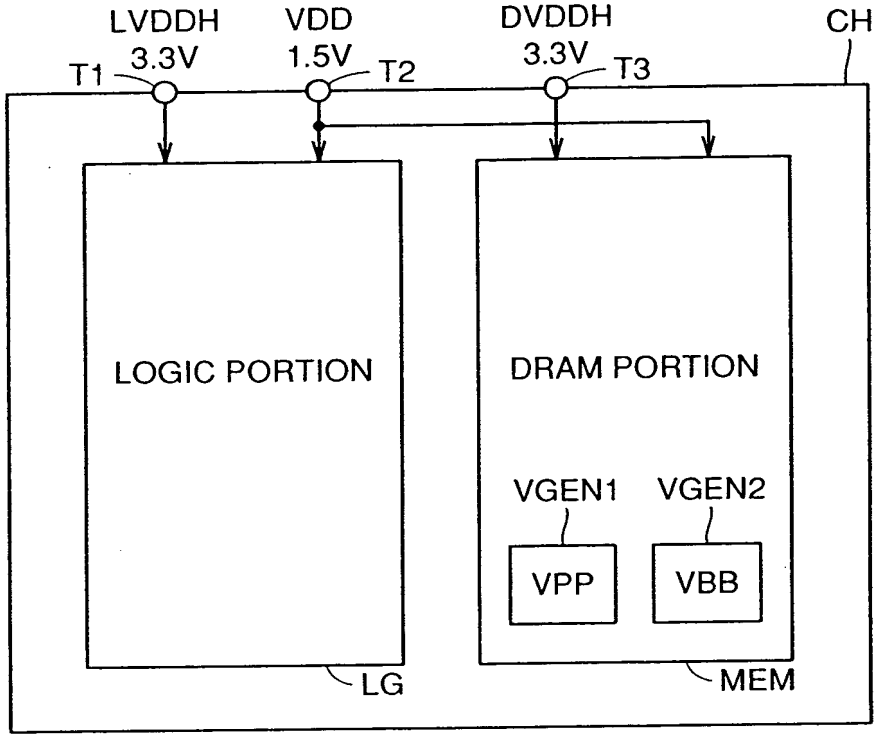
LVDDH
3.3V
VDD
1.5V
DVDDH
3.3V
CH
T1
T2
T3
LOGIC PORTION
DRAM PORTION
VGEN1
VGEN2
VPP
VBB
LG
MEM

FIG.10

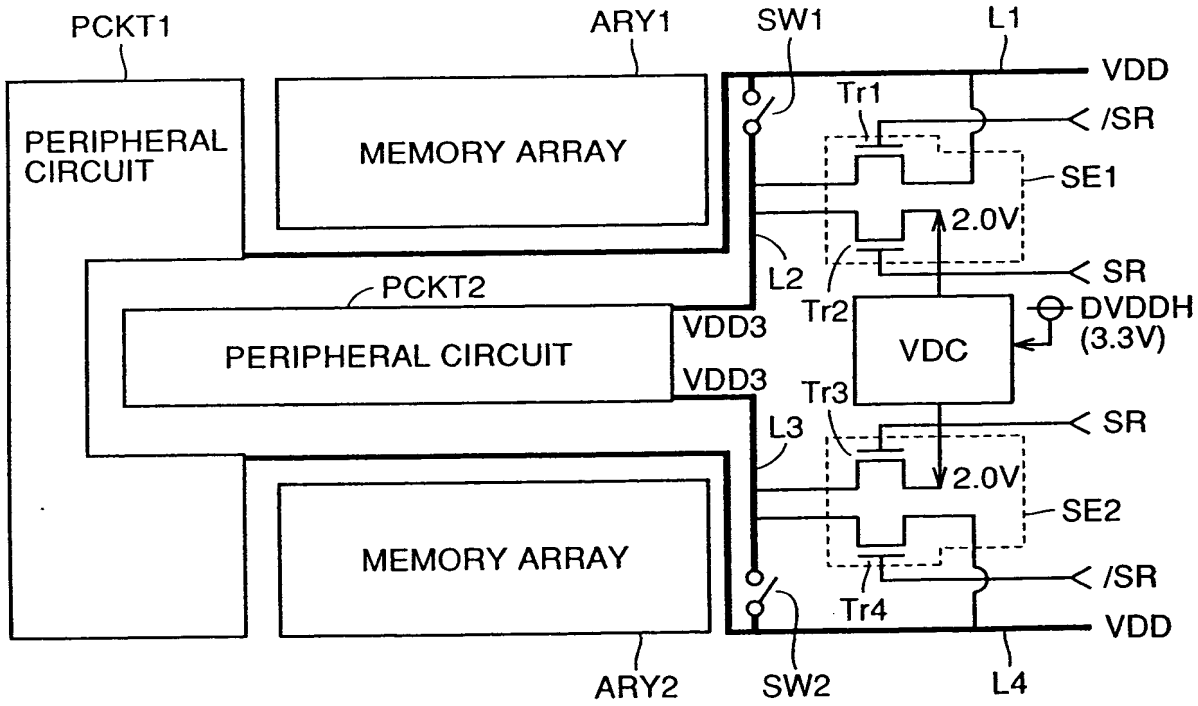
PCKT1
ARY1
SW1
L1
VDD
PERIPHERAL CIRCUIT
MEMORY ARRAY
Tr1
/SR
SE1
2.0V
SR
L2
PCKT2
Tr2
DVDDH
(3.3V)
VDD3
PERIPHERAL CIRCUIT
VDC
VDD3
Tr3
SR
L3
2.0V
SE2
MEMORY ARRAY
/SR
Tr4
VDD
ARY2
SW2
L4

FIG.11

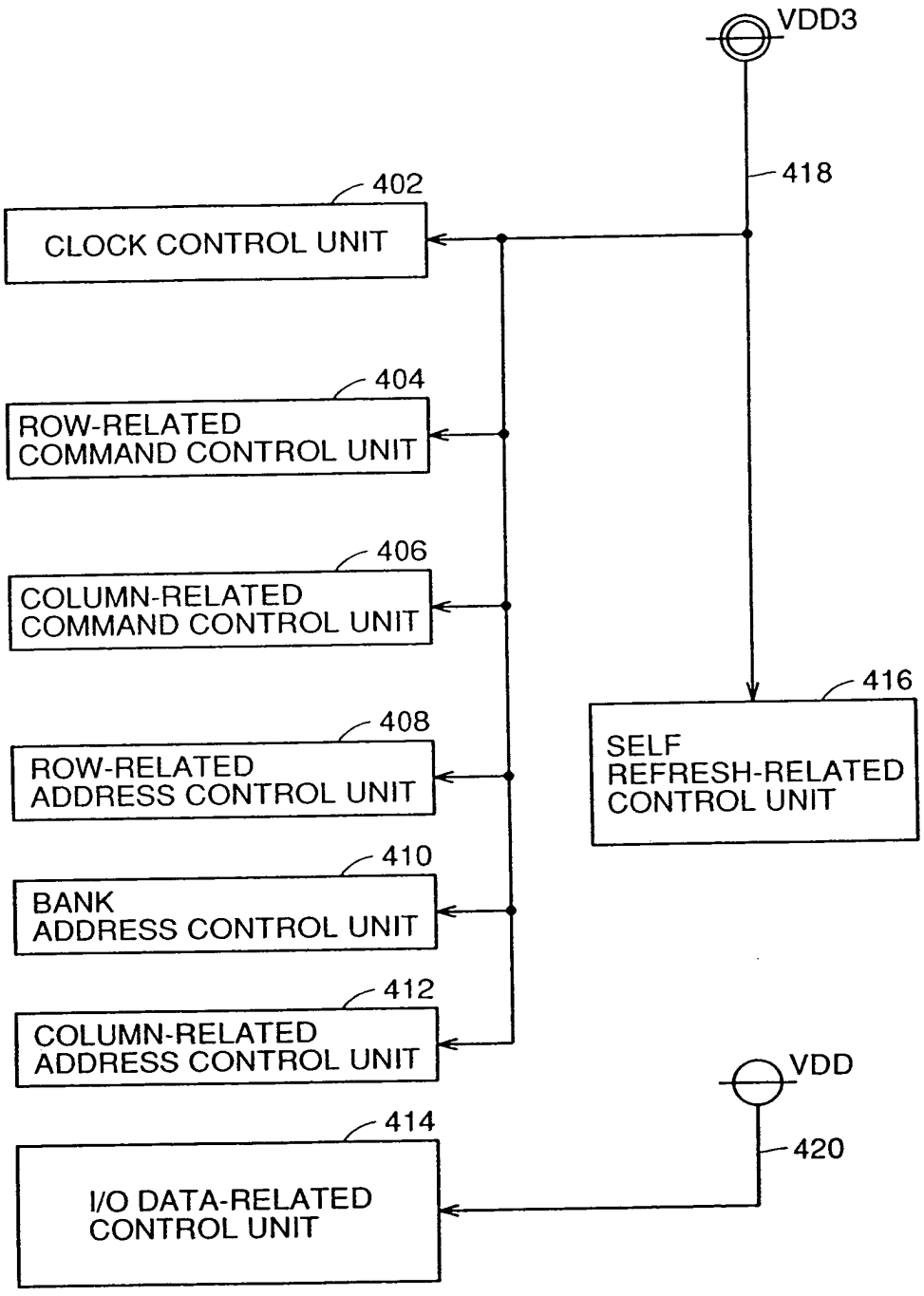
VDD3
418
402
CLOCK CONTROL UNIT
404
ROW-RELATED
COMMAND CONTROL UNIT
406
COLUMN-RELATED
COMMAND CONTROL UNIT
408
ROW-RELATED
ADDRESS CONTROL UNIT
410
BANK
ADDRESS CONTROL UNIT
412
COLUMN-RELATED
ADDRESS CONTROL UNIT
414
I/O DATA-RELATED
CONTROL UNIT
416
SELF
REFRESH-RELATED
CONTROL UNIT
VDD
420

FIG. 12

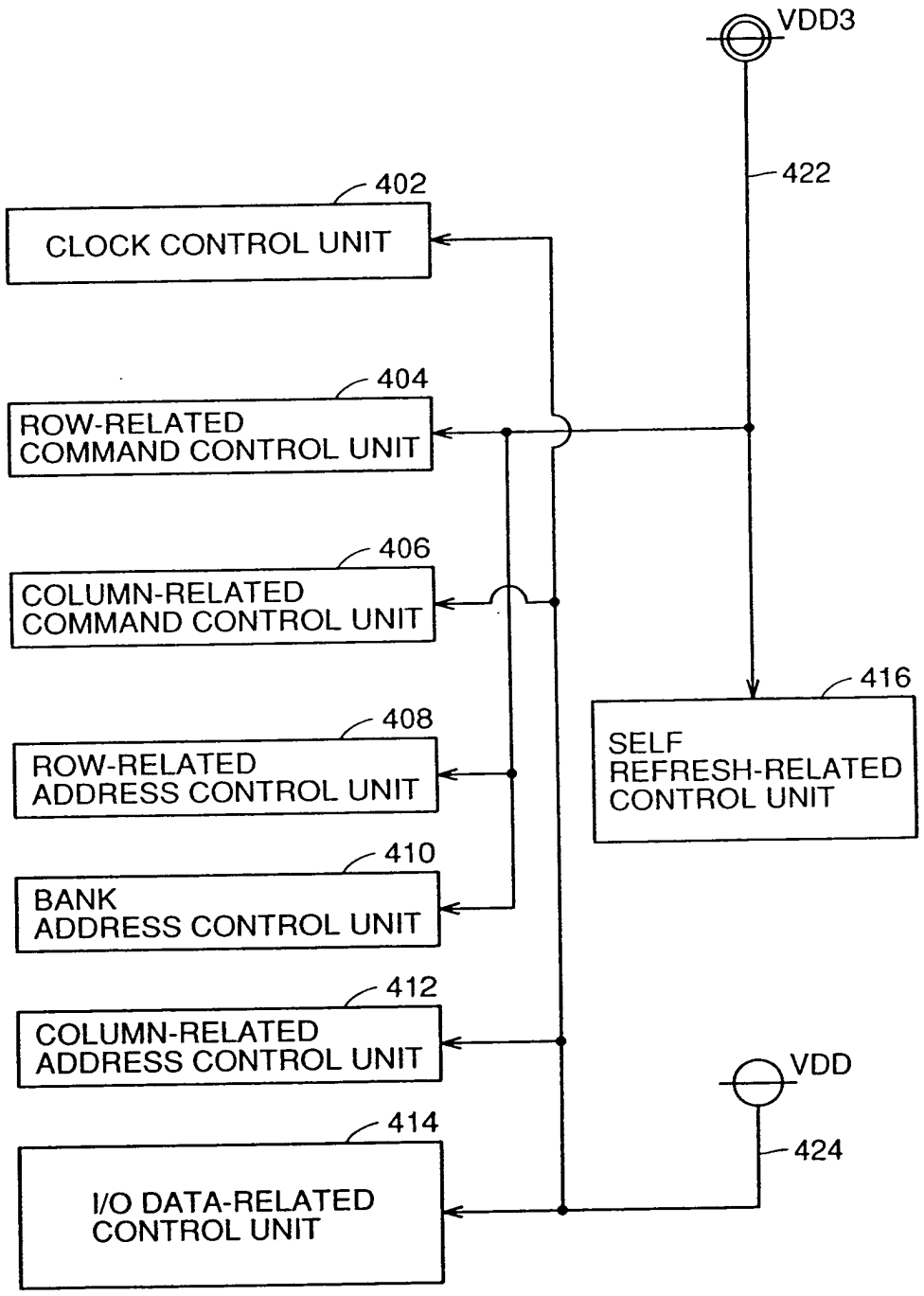
VDD3
422
402
CLOCK CONTROL UNIT
404
ROW-RELATED
COMMAND CONTROL UNIT
406
COLUMN-RELATED
COMMAND CONTROL UNIT
416
SELF
REFRESH-RELATED
CONTROL UNIT
408
ROW-RELATED
ADDRESS CONTROL UNIT
410
BANK
ADDRESS CONTROL UNIT
412
COLUMN-RELATED
ADDRESS CONTROL UNIT
VDD
414
424
I/O DATA-RELATED
CONTROL UNIT

FIG.13

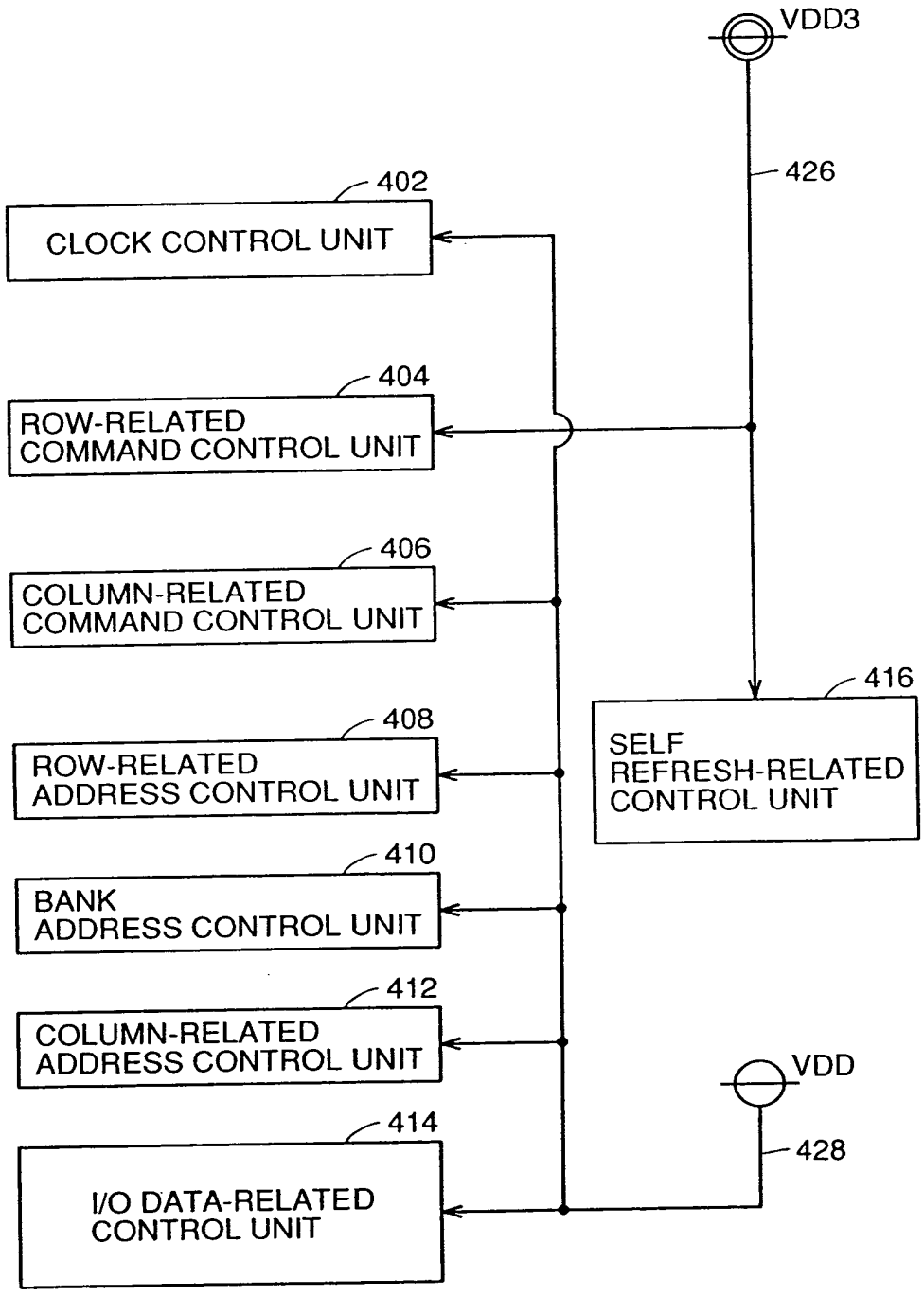
VDD3
426
402
CLOCK CONTROL UNIT
404
ROW-RELATED
COMMAND CONTROL UNIT
406
COLUMN-RELATED
COMMAND CONTROL UNIT
416
SELF
REFRESH-RELATED
CONTROL UNIT
408
ROW-RELATED
ADDRESS CONTROL UNIT
410
BANK
ADDRESS CONTROL UNIT
412
COLUMN-RELATED
ADDRESS CONTROL UNIT
VDD
414
428
I/O DATA-RELATED
CONTROL UNIT

FIG. 14

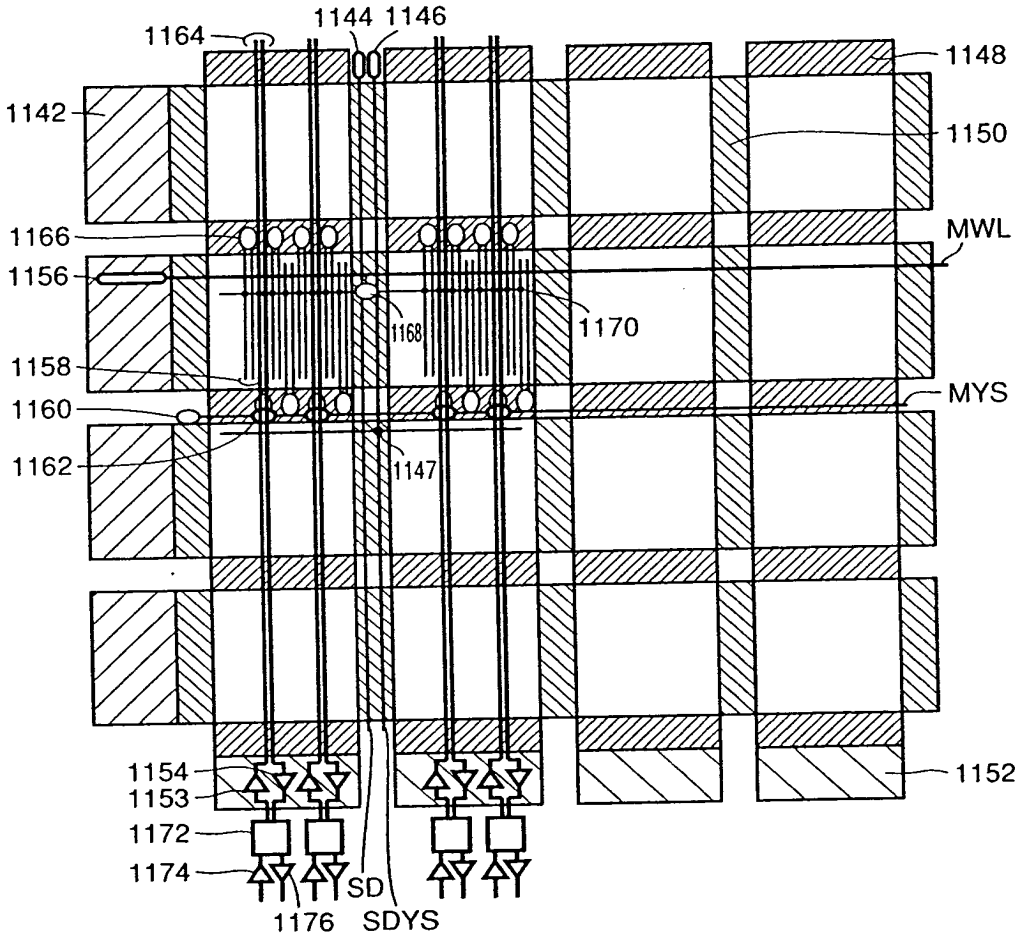
1164
1144
1146
1148
1142
1150
1166
MWL
1156
1168
1170
1158
MYS
1160
1162
1147
1154
1153
1152
1172
1174
SD
1176
SDYS

FIG. 15

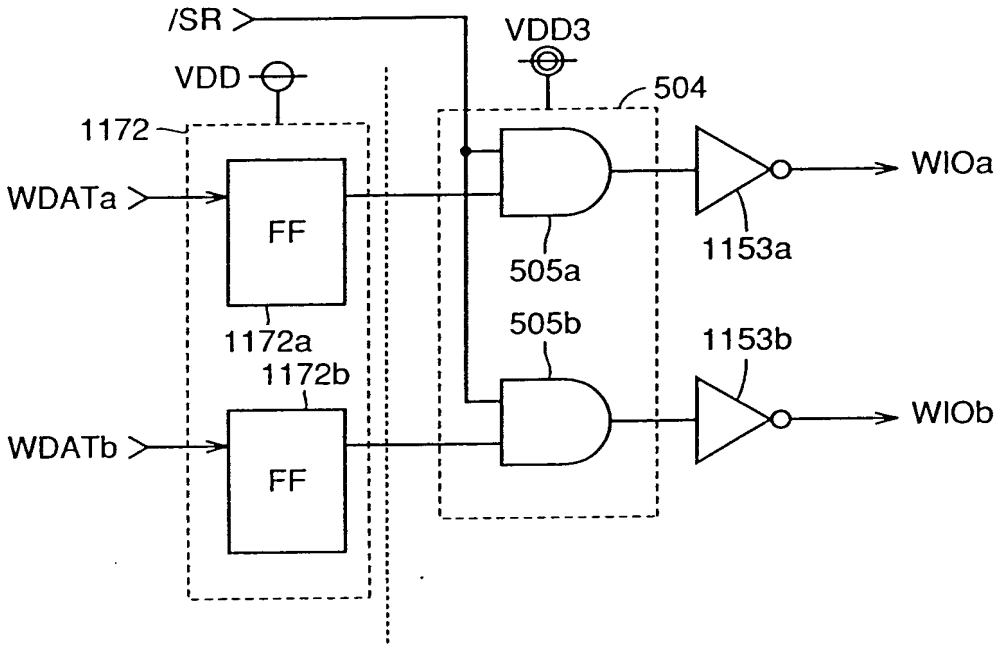
/SR
VDD3
VDD
504
1172
WDATa
FF
WIOa
505a
1153a
1172a
505b
1153b
1172b
WDATb
FF
WIOb

FIG. 16

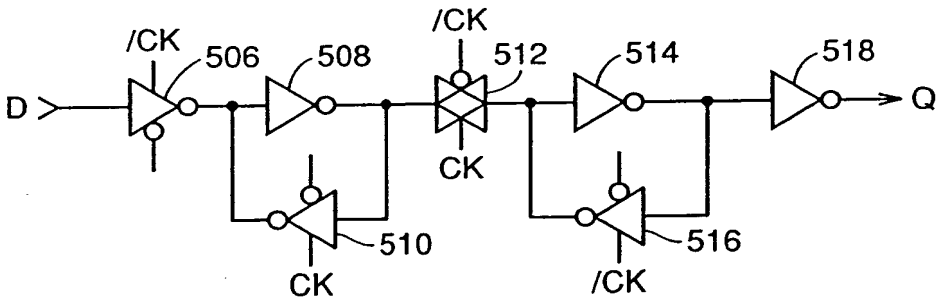
/CK
/CK
506
508
512
514
518
D
Q
CK
510
516
CK
/CK

FIG.17

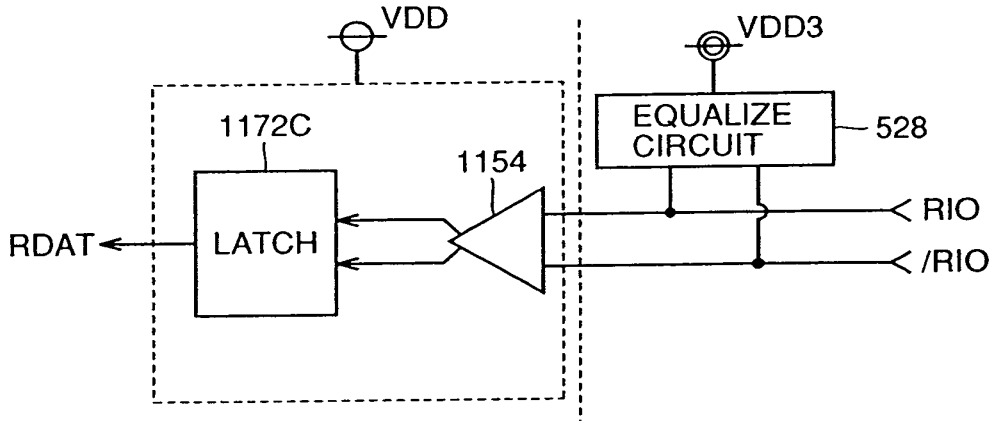
VDD
VDD3
1172C
EQUALIZE CIRCUIT
528
1154
RDAT
LATCH
RIO
/RIO

FIG.18

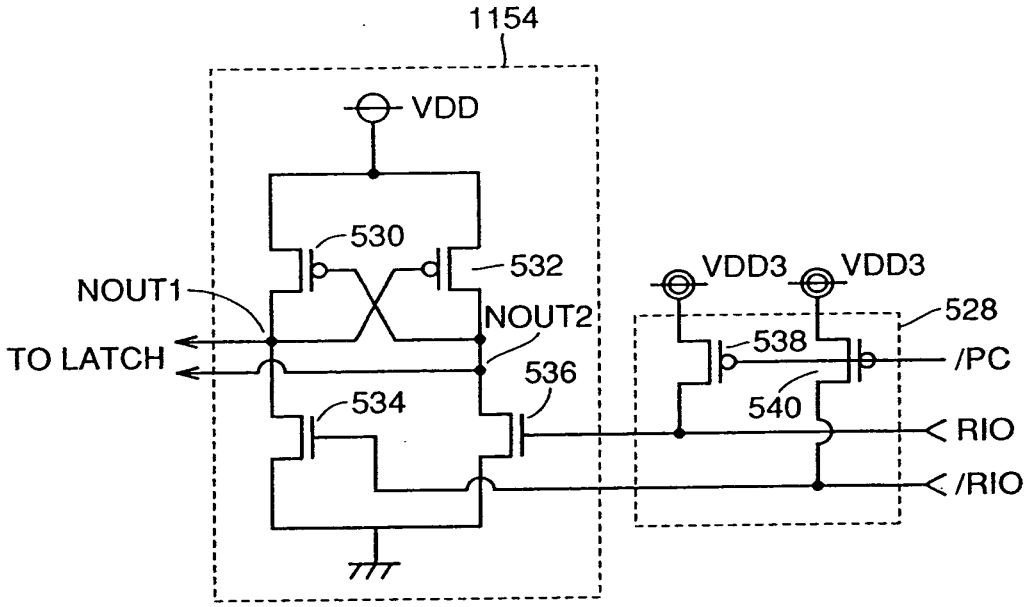
1154
VDD
530
532
VDD3
VDD3
NOUT1
NOUT2
528
538
TO LATCH
/PC
536
534
540
RIO
/RIO

FIG. 19

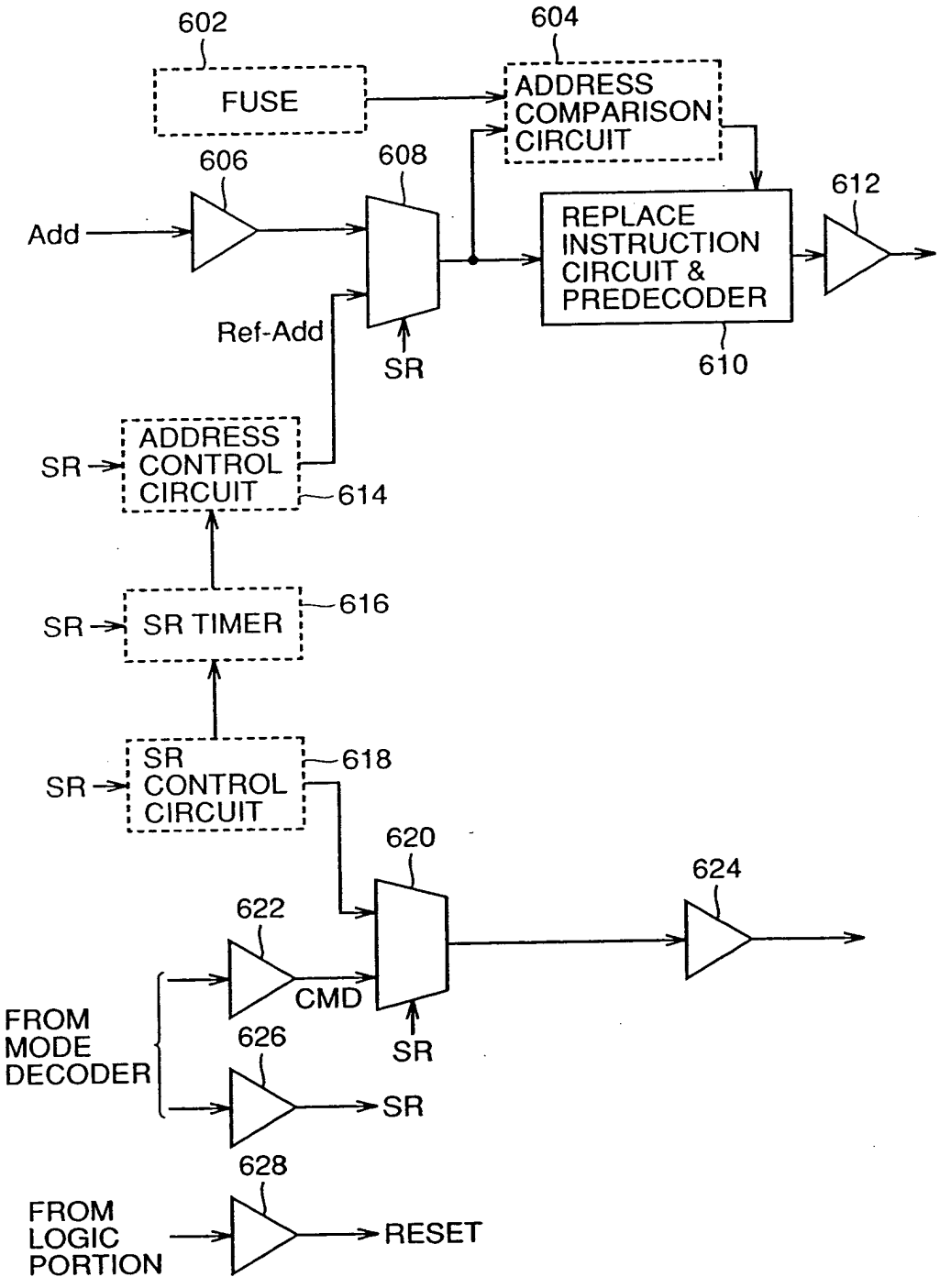
602
FUSE
604
ADDRESS COMPARISON CIRCUIT
606
608
612
Add
REPLACE INSTRUCTION CIRCUIT & PREDECODER
Ref-Add
SR
610
SR
ADDRESS CONTROL CIRCUIT
614
SR
SR TIMER
616
SR
SR CONTROL CIRCUIT
618
620
624
622
CMD
FROM MODE DECODER
626
SR
628
FROM LOGIC PORTION
RESET

FIG. 20

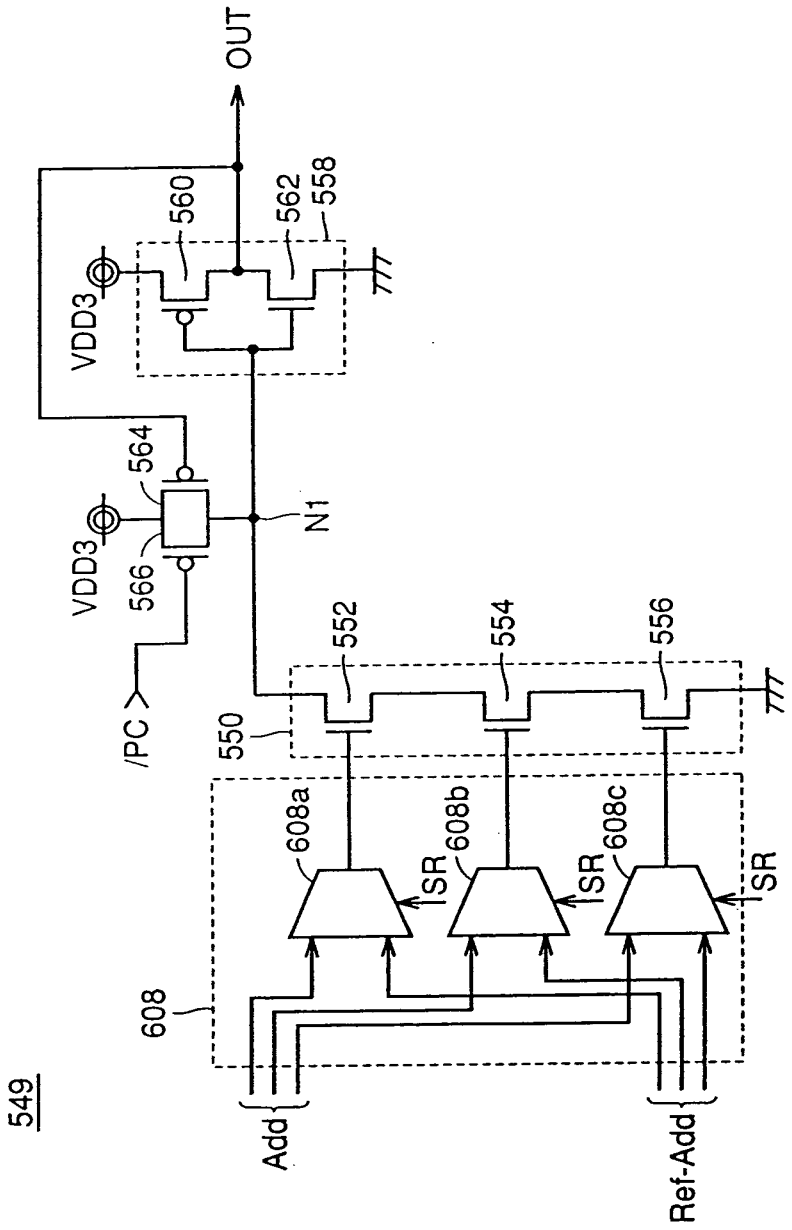
549
608
608a
608b
608c
SR
SR
SR
Add
Ref-Add
550
552
554
556
/PC
VDD3
566
564
N1
VDD3
560
562
558
OUT

FIG.21

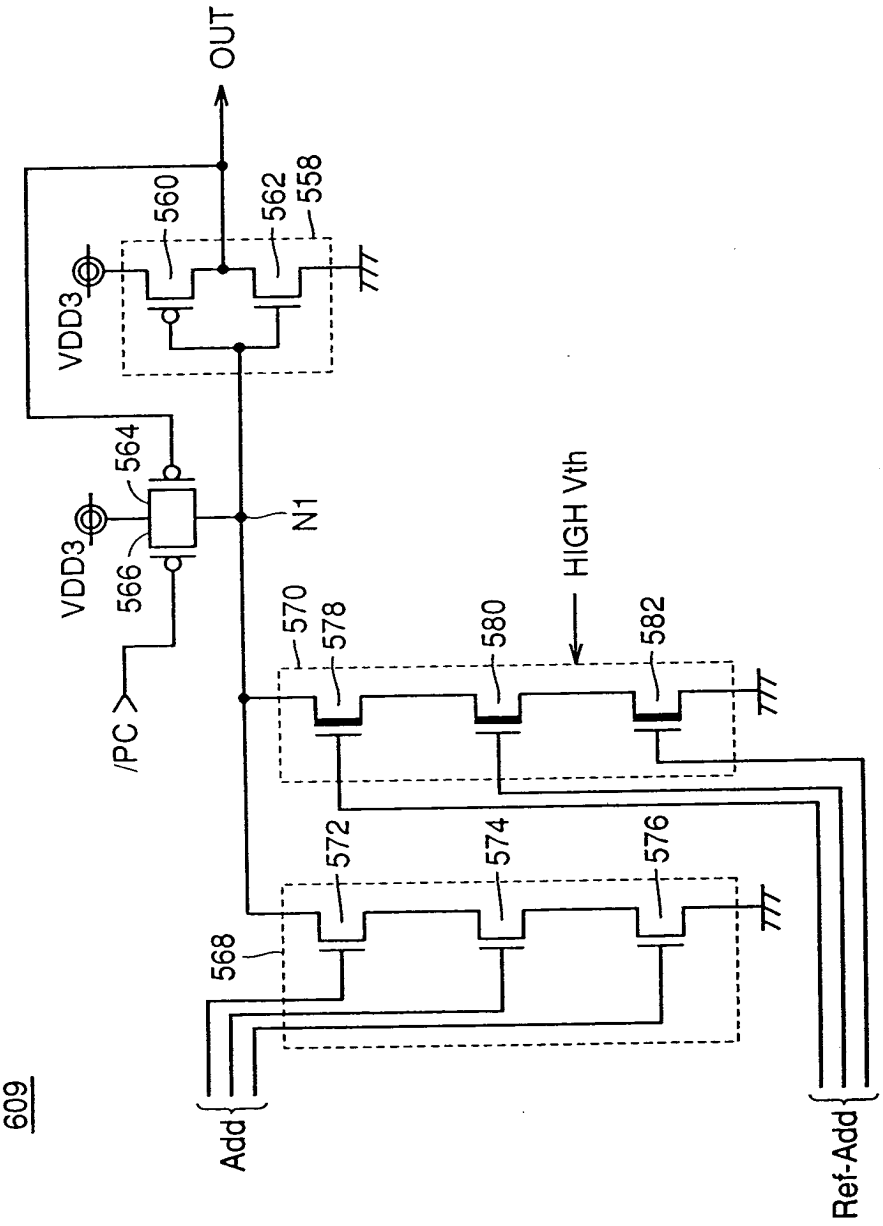
609
OUT
VDD3
560
562
558
564
VDD3
566
N1
/PC
570
578
580
582
HIGH Vth
572
574
576
568
Add
Ref-Add

FIG.22

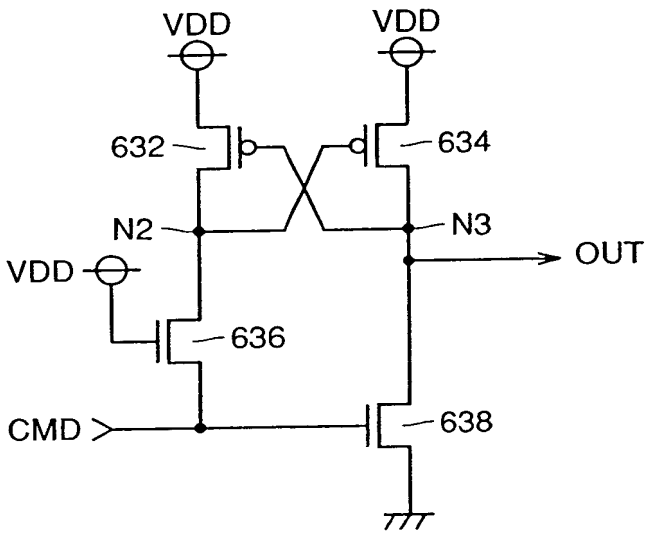
VDD
VDD
632
634
N2
N3
OUT
VDD
636
CMD
638

FIG.23

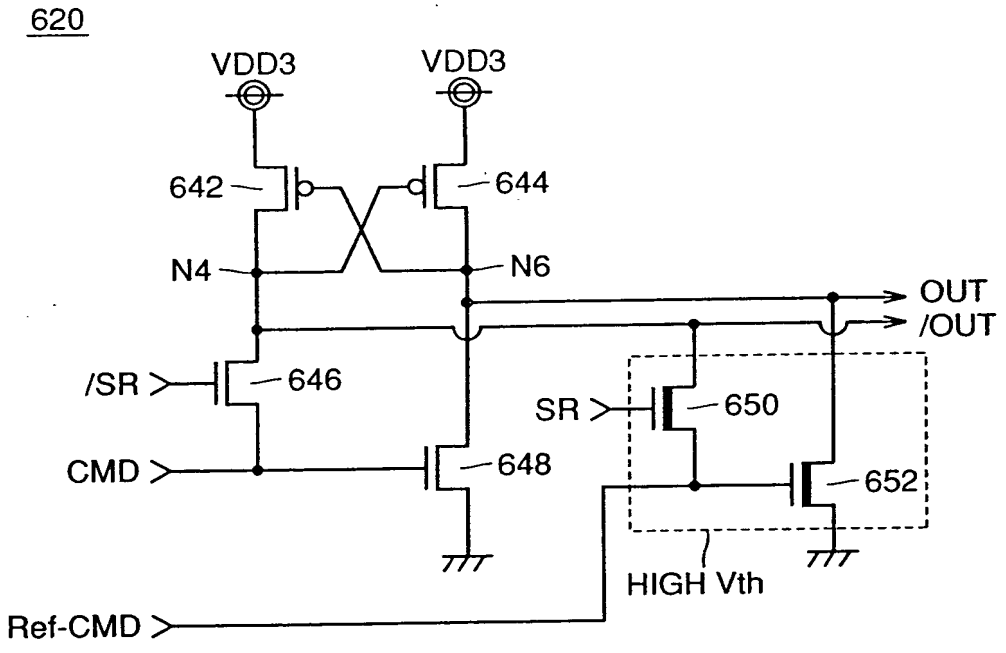
620
VDD3
VDD3
642
644
N4
N6
OUT
/OUT
/SR
646
SR
650
CMD
648
652
HIGH Vth
Ref-CMD

FIG. 24

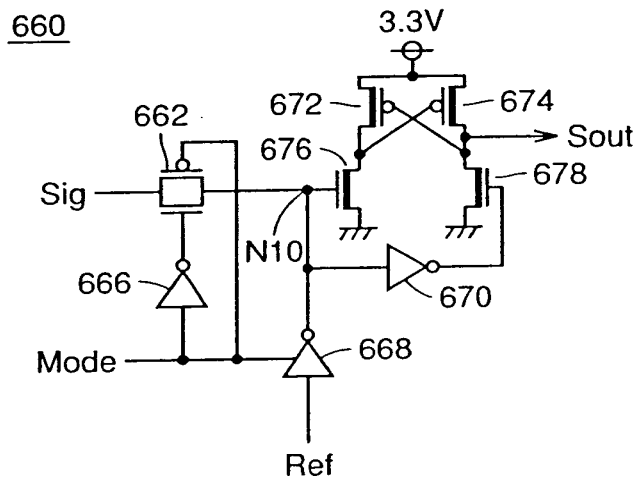
660
3.3V
672
674
662
Sout
676
678
Sig
N10
666
670
Mode
668
Ref

FIG. 25

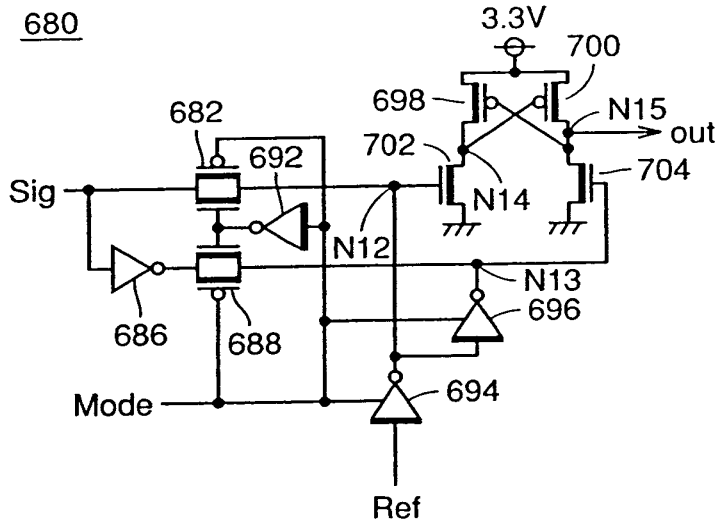
680
3.3V
700
698
682
N15
out
692
702
704
Sig
N14
N12
N13
696
686
688
Mode
694
Ref

FIG. 26

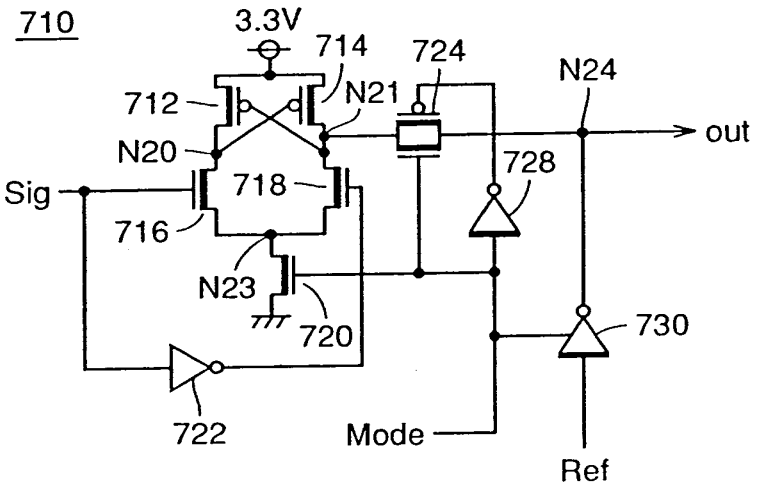
710
3.3V
714
724
N24
712
N21
out
N20
728
Sig
718
716
N23
720
730
722
Mode
Ref

FIG. 27

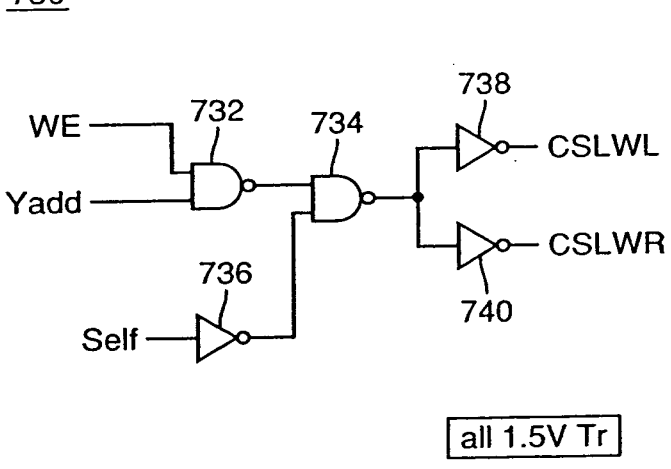
730
738
WE
732
734
CSLWL
Yadd
CSLWR
736
740
Self
all 1.5V Tr

FIG.28

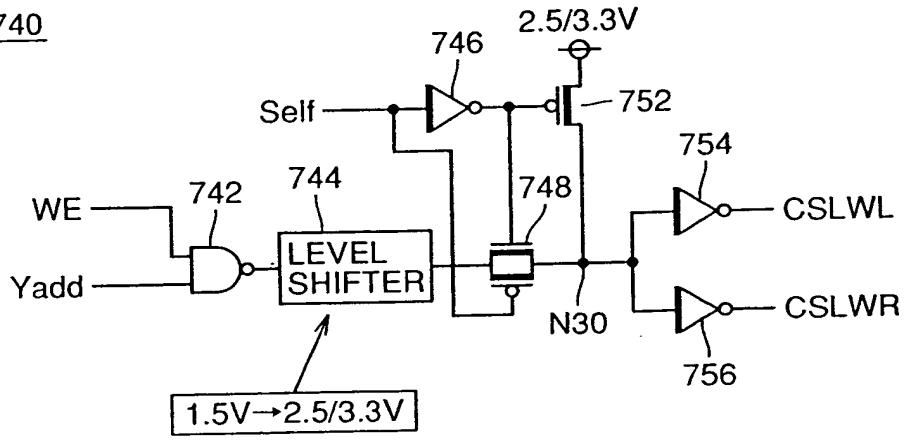
740
746
2.5/3.3V
Self
752
754
WE
742
744
748
CSLWL
Yadd
LEVEL SHIFTER
N30
CSLWR
756
1.5V→2.5/3.3V

FIG.29

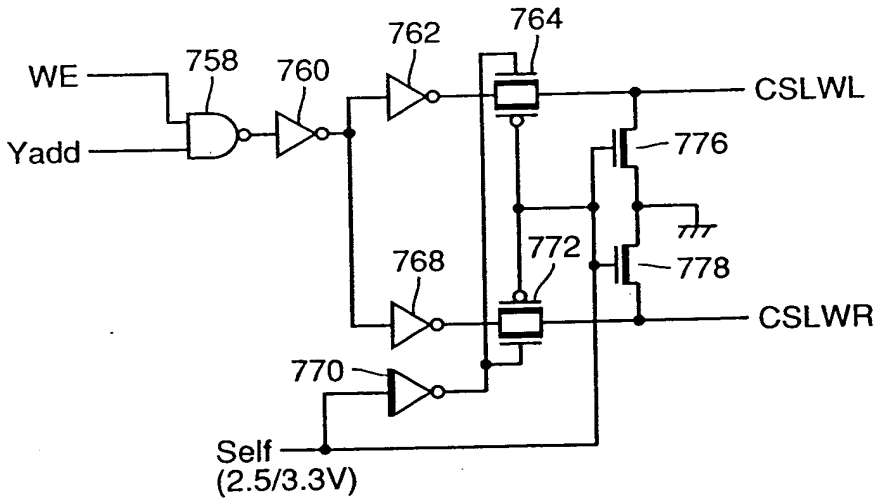
757
762
764
WE
758
760
CSLWL
776
Yadd
772
768
778
CSLWR
770
Self
(2.5/3.3V)

FIG.30

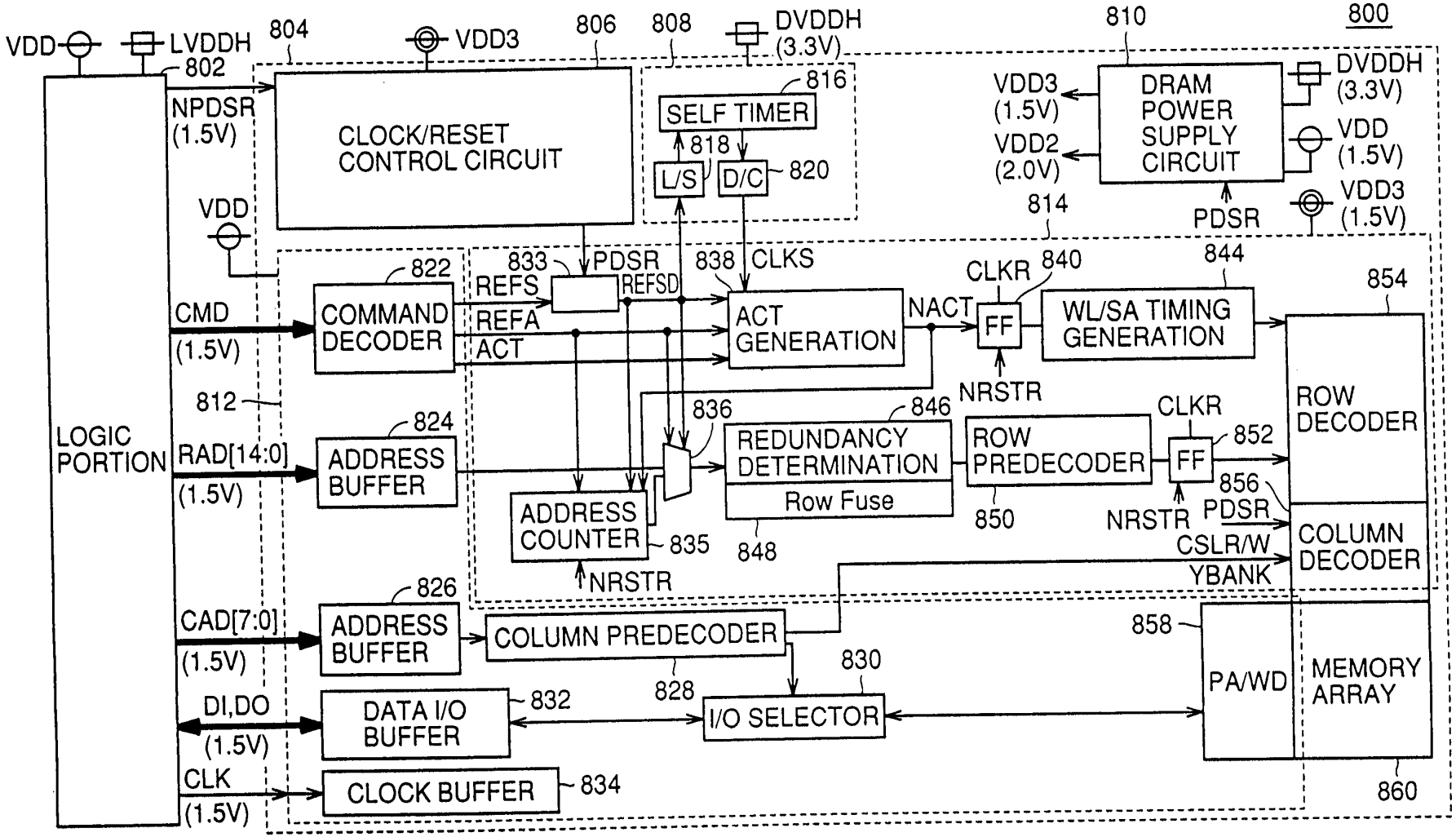
VDD
LVDDH
802
804
VDD3
806
808
DVDDH
(3.3V)
810
800
NPDSR
(1.5V)
CLOCK/RESET
CONTROL CIRCUIT
SELF TIMER
816
818
L/S
D/C
820
VDD3
(1.5V)
VDD2
(2.0V)
DRAM
POWER
SUPPLY
CIRCUIT
DVDDH
(3.3V)
VDD
(1.5V)
VDD3
(1.5V)
PDSR
814
VDD
822
833
PDSR
838
CLKS
CLKR
840
844
854
CMD
(1.5V)
COMMAND
DECODER
REFS
REFSD
REFA
ACT
ACT
GENERATION
NACT
FF
WL/SA TIMING
GENERATION
NRSTR
812
836
846
CLKR
ROW
DECODER
LOGIC
PORTION
RAD[14:0]
(1.5V)
824
ADDRESS
BUFFER
REDUNDANCY
DETERMINATION
Row Fuse
ROW
PREDECODER
FF
852
856
ADDRESS
COUNTER
835
848
850
NRSTR
PDSR
CSLR/W
YBANK
COLUMN
DECODER
NRSTR
826
CAD[7:0]
(1.5V)
ADDRESS
BUFFER
COLUMN PREDECODER
858
830
828
DI,DO
(1.5V)
DATA I/O
BUFFER
832
I/O SELECTOR
PA/WD
MEMORY
ARRAY
CLK
(1.5V)
CLOCK BUFFER
834
860

FIG.31

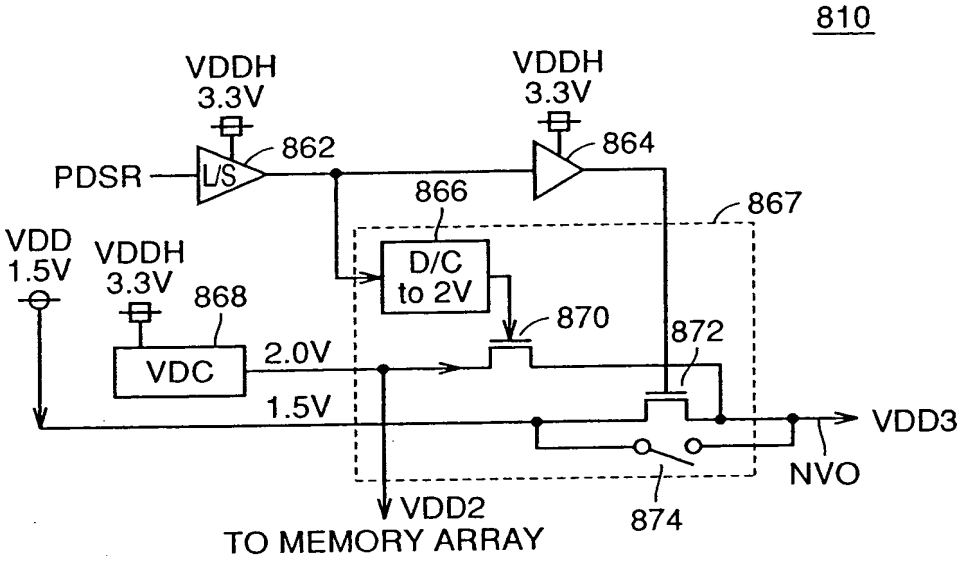
810
VDDH
3.3V
VDDH
3.3V
862
864
PDSR
L/S
866
867
VDD
1.5V
VDDH
3.3V
868
D/C
to 2V
870
872
VDC
2.0V
1.5V
VDD3
NVO
VDD2
TO MEMORY ARRAY
874

FIG.32

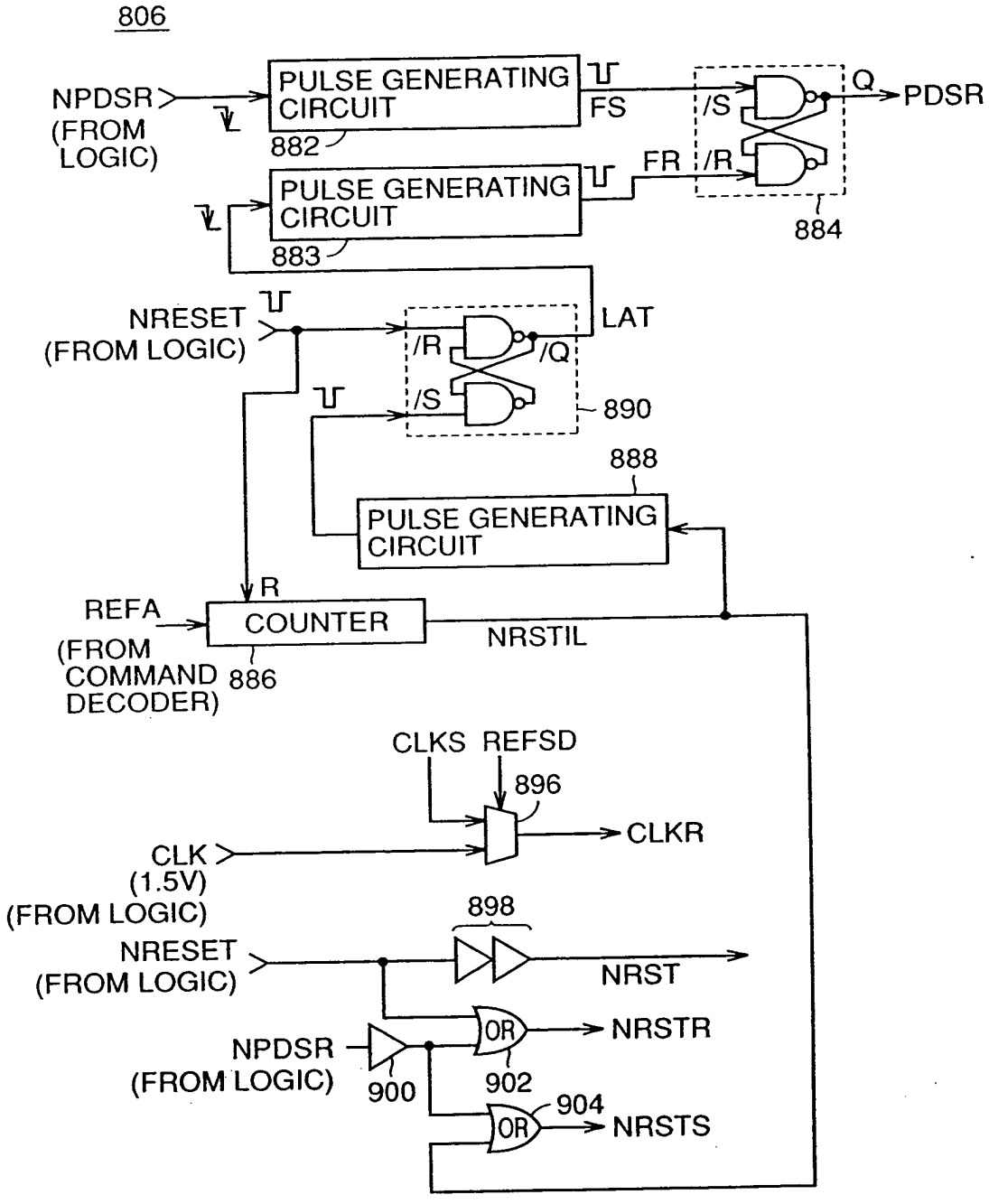
806
NPDSR
(FROM LOGIC)
PULSE GENERATING CIRCUIT
882
FS
PULSE GENERATING CIRCUIT
883
FR
/S
/R
Q
PDSR
884
NRESET
(FROM LOGIC)
/R
/Q
/S
LAT
890
888
PULSE GENERATING CIRCUIT
R
REFA
(FROM COMMAND DECODER)
COUNTER
886
NRSTIL
CLKS
REFSD
896
CLK
(1.5V)
(FROM LOGIC)
CLKR
898
NRESET
(FROM LOGIC)
NRST
OR
NRSTR
NPDSR
(FROM LOGIC)
900
902
904
OR
NRSTS

FIG.33

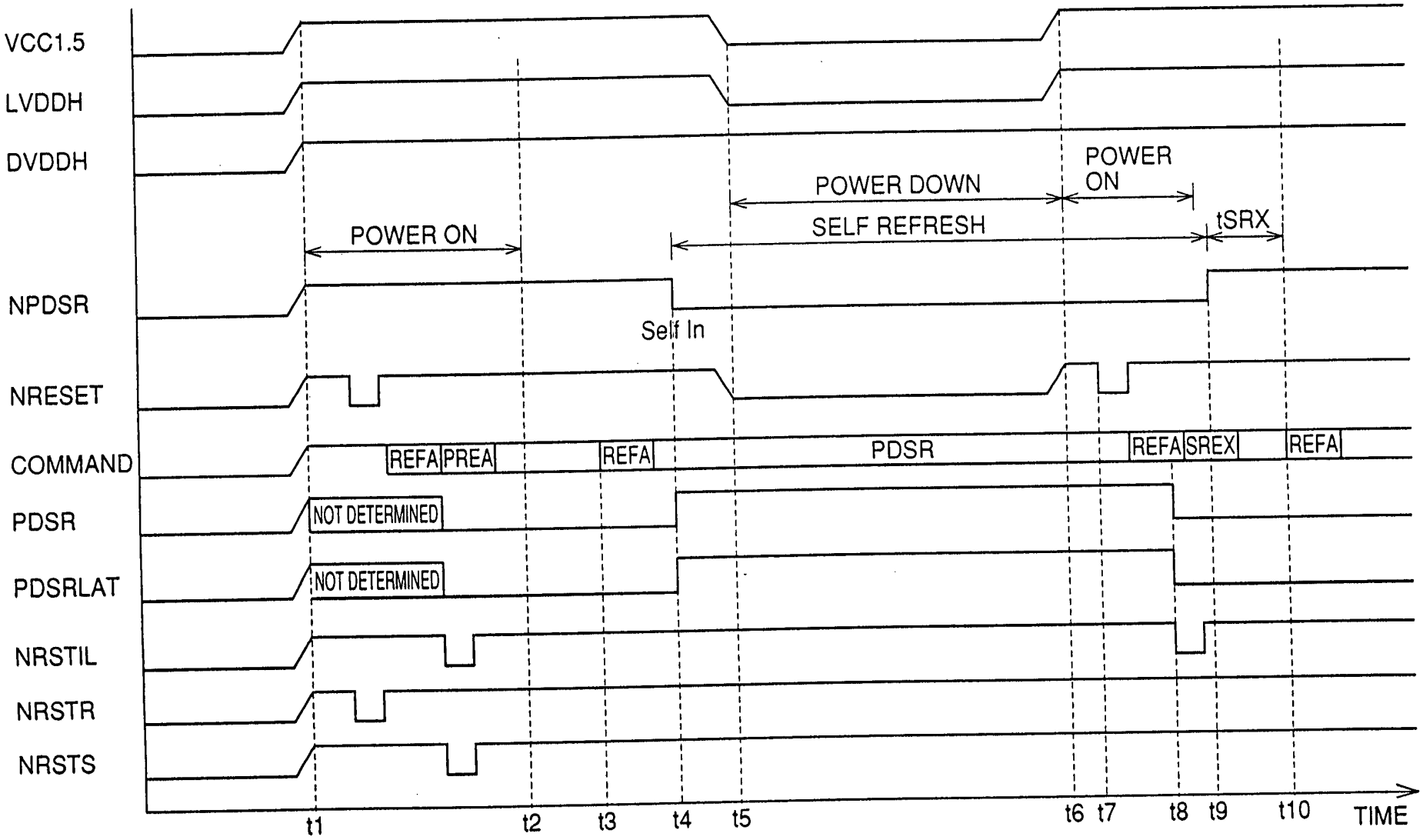
VCC1.5
LVDDH
DVDDH
POWER ON
POWER DOWN
SELF REFRESH
POWER ON
tSRX
NPDSR
Self In
NRESET
COMMAND
REFA
PREA
REFA
PDSR
REFA
SREX
REFA
PDSR
NOT DETERMINED
PDSRLAT
NOT DETERMINED
NRSTIL
NRSTR
NRSTS
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
TIME

FIG.34

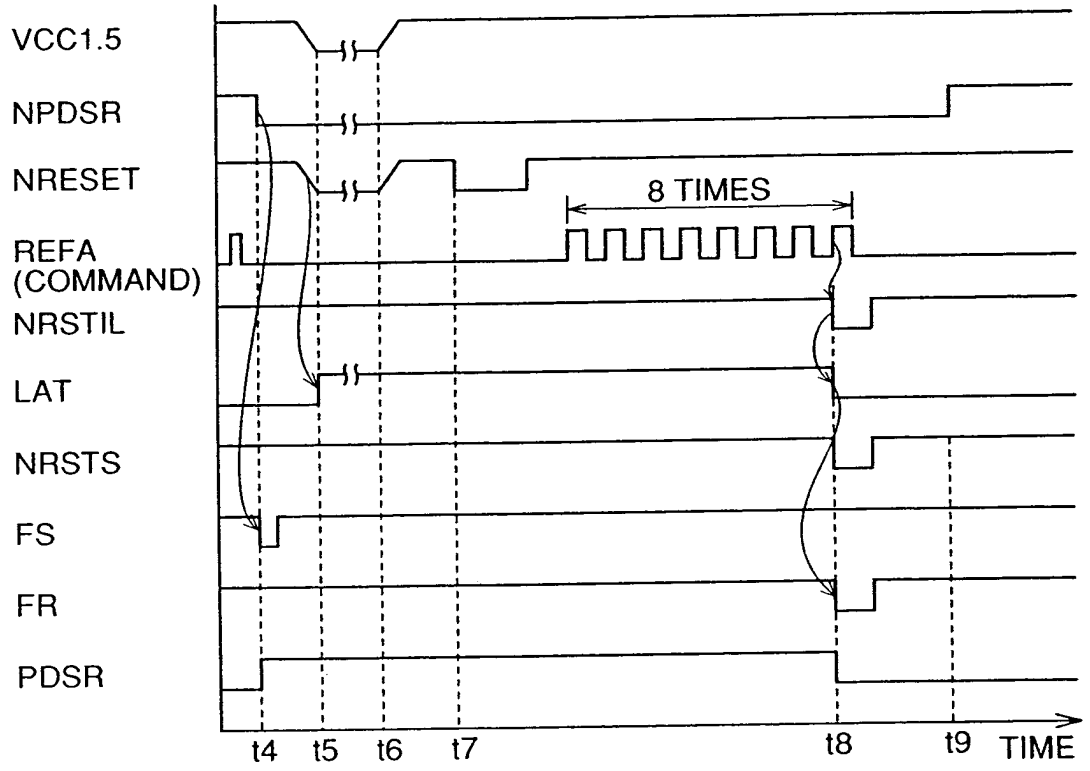
VCC1.5
NPDSR
NRESET
8 TIMES
REFA
(COMMAND)
NRSTIL
LAT
NRSTS
FS
FR
PDSR
t4
t5
t6
t7
t8
t9
TIME

FIG.35 PRIOR ART

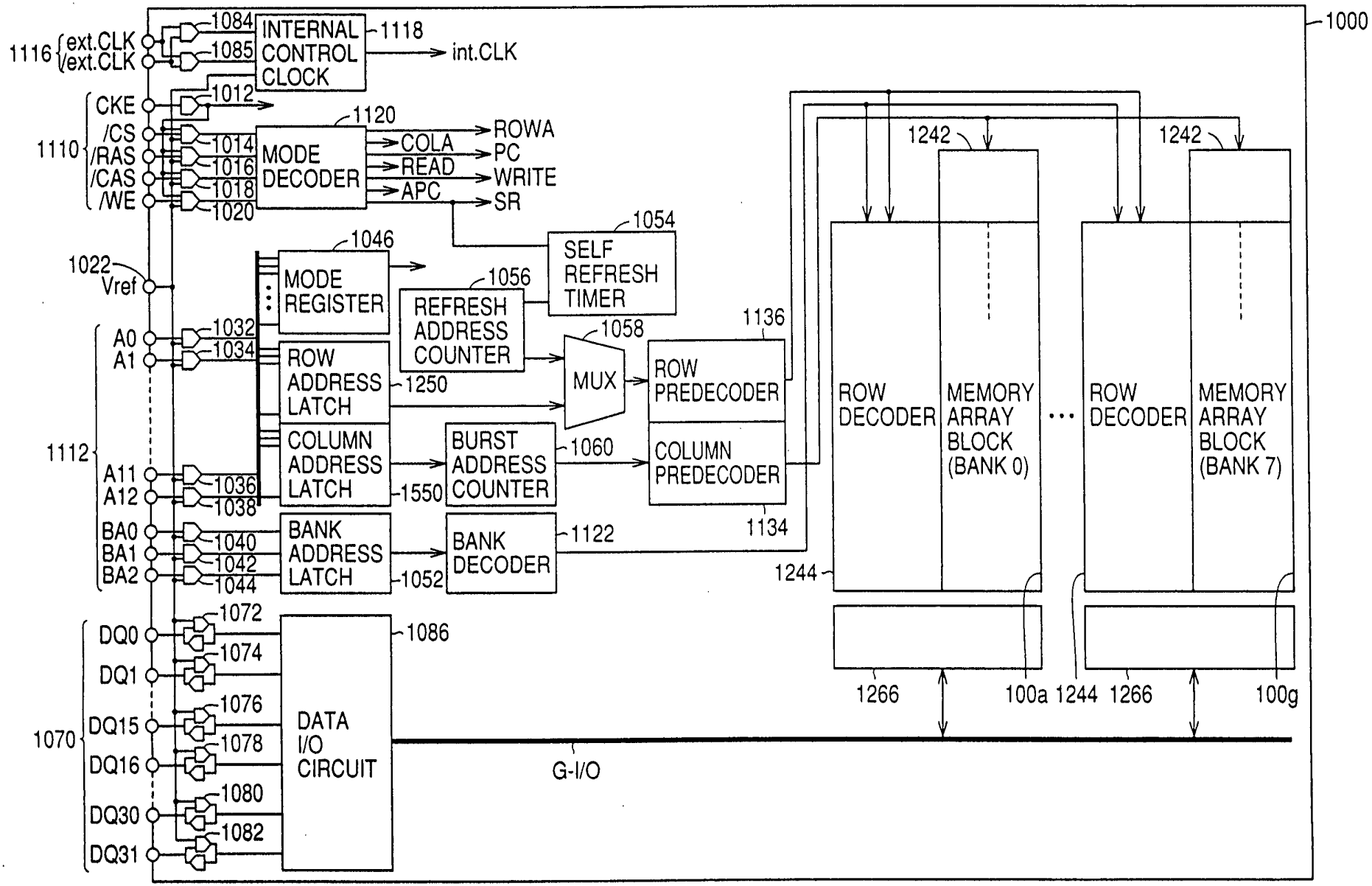

FIG.36 PRIOR ART

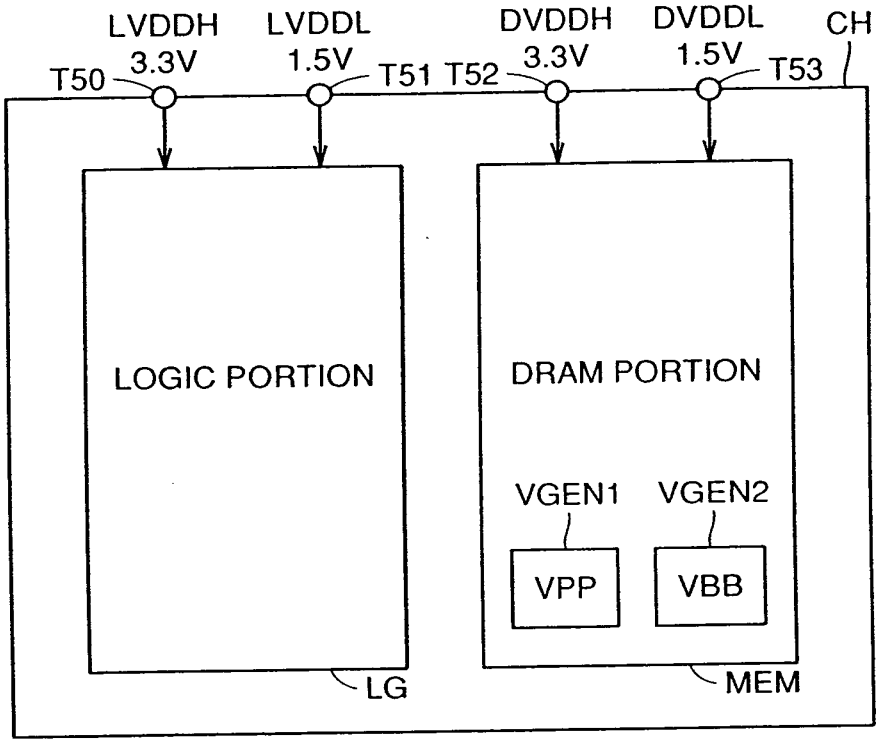

FIG.37 PRIOR ART